Control architectures for synchronized parallel inverters

Prima Electro is a strategic EMS partner in high-tech sectors such as railway, energy and industrial automation. For over forty years, we have been converting ideas into full-custom embedded products, becoming the reference point for all those companies wishing to improve the features and performances of their systems with industrial-grade solutions. Always at the cutting edge of technology in power and control electronics design and production, Prima Electro offers support from the concept and preliminary analysis through the qualification and production stage, supervising the whole manufacturing process. Our business model can be summed up in the acronym DOTS (Dedicated Off The Shelf), because we are able to offer custom "end-to-end" turnkey solutions with a fast time-to-market and competitive costs.

Background:

When increasing the inverter power, some challenges suddenly appear, leading to an increase in end product cost and complexity. For example, the thermal design may require special parts or materials, or the semiconductor switches may not be available in standard packages, losing the interchangeability. Some power sizes become more optimized and attractive than other. It would be desirable to build a large power inverter by combining several optimized-size inverters in parallel. To avoid large and expensive inductors at the output of each inverter, each inverter output stage must switch precisely at the same time.
This leads to an architecture with a single, centralized, control unit implementing the motor control algorithm, and multiple Power units switching in parallel and synchronously.
A communication channel must be established between the Control unit and all the Power units. This communication channel must carry the timing and the duty cycle information (to ensure synchronization).
To avoid the effects of the noise, caused by the power switching, on the communication channel between the Control unit and the Power units, an isolated Master-Slave communication scheme is necessary.

Type of work: Master Thesis

The goal of the thesis is to investigate the architectures using state-of-the-art or customized techniques for isolated communication Master-Slaves with very low propagation delay or, at least, with propagation delay compensation.
Examples are:

- Industrial Ethernet fieldbus, like EtherCAT (copper based)
- galvanically isolated multi-wire serial lines (copper based)
- optical fiber serial connections (fiber based)

Expected tasks:

- Analysis of scalable architectures with single centralized Control unit and multiple Power units connected in parallel. Analysis of their requirements for the synchronization and communication channel. (10% of time)
- Literature survey of the state-of-the-art techniques for Master-Slaves communication, suitable for the requirements identified above. (10% of time)
- Analysis of custom techniques for Master-Slaves communication, suitable for the requirements identified above. (10% of time)
- Experimental testing of timing and throughput with Evaluation boards and Control unit. (20% of time)
- Experimental testing on an industrial converter (40% of time)
- Documentation of all the activities. (10% of time)

Requirements:

- Background on digital communication electronics and protocols.
- Background on noise issues with communication.
- Basic knowledge of power electronics converters principles and topologies
- Basic knowledge of analog circuit design
- Analytical skills
- Firmware programming skill (C language)
- FPGA programming skill (VHDL or Verilog) is a plus.

Duration: 6-9 months

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The master thesis project will be carried out at Prima Electro S.p.A.
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